GOVERNMENT OF KERALA
DEPARTMENT OF TECHNICAL EDUCATION
COLLEGE OF ENGINEERING TRIVANDRUM

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**Dated: September 03, 2024**

## Walkin Interview for the post of Junior Research Fellow (1)

Applications are invited from highly motivated candidates for the positions of Junior Research Fellows (JRFs) in sponsored project of Ministry of Electronics & Information Technology (MeitY) under Chips to Startup (C2S) initiative for the project entitled "**A SHAKTI CPU based Smart Vision System on Chip (SoC)**" to be implemented jointly by College of Engineering Trivandrum and M/s Netrasemi Private Limited, Thiruvananthapuram.

**Aim of the Project**: MeitY recently has announced a semiconductor "Chips to Startup (C2S)" program that not only aims at developing Specialized Manpower in VLSI/Embedded System Design domain but also addresses each entity of the Electronics value chain via Specialized Manpower training, creation of reusable IPs repository, Design of application-oriented Systems/ASICs/FPGAs and deployment by academia/ R&D organization by way of leveraging the expertise available at Start-ups/MSMEs. A joint proposal by College of Engineering Trivandrum (CET) and Netrasemi Private Limited has been selected for the program with central funding under Category-1 (4.7 Crore) for developing an indigenous RISC-V AI/ML chip. The selected candidates will get an opportunity to work on this prestigious project.

**Duration**: Initial appointment is for one year (contract basis) which is extendable up to the duration of the project.

**Number of vacancies: 1**

**Eligibility criteria:**

**Junior Research Fellow: VLSI Design**

**Scale of pay: Rs. 37,000/- per month.**

**Essential:** BTech/BE in EC/EE/AE/EI with valid GATE score.

**Desirable**: MTech/ME in EC/EE/AE/EI, Industry experience of 0-2 years/ Very good knowledge in RTL coding, computer-architecture, SoC design, test and debug. Experience in ASIC backend flow using Cadence/Synopsys EDA tools.

**OR**

**Project Associate: VLSI Design**

**Scale of pay: Rs. 25,000/- per month.**

**Essential:** BTech/BE in EC/EE/AE/EI

**Desirable**: MTech/ME in EC/EE/AE/EI, Industry experience of 0-2 years/ Very good knowledge in RTL coding, computer-architecture, SoC design, test and debug. Experience in ASIC backend flow using Cadence/Synopsys EDA tools.

**How to apply?**

Please visit www.cet.ac.in. Go to News session and click on Walk-in Interview for the post of JRF/Project Associate for C2S, Central Government funded project.

Interested applicants are requested to download the **application form** and fill in the details.

Next, register through the **registration** link provided. You need to upload the completed application form with the file name as your full name.

Please bring the completed application form and original certificates for verification. You need to submit the application form and a self-attested copy of all relevant documents before attending the interview.

Following original documents are required

1. Completed application form
2. B Tech Degree Certificate
3. M Tech Degree Certificate
4. Documents ($10^{th}$ / Plus 2 certificates, Aadhaar Card, etc.) for verifying name, date of birth and address.

***The walk-in interview will be held at Department of Electronics & Communication Engineering, College of Engineering Trivandrum, on $11^{th}$ September, 2024. The candidates should report to the department before 09.30 am on $11^{th}$ September, 2024.***