COLLEGE OF ENGINEERING TRIVANDRUM
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Advertisement for the post of Junior Research Fellow (07)

Applications are invited from highly motivated candidates for the positions of Junior Research Fellows (JRFs) in sponsored project of Ministry of Electronics & Information Technology (MeitY) under Chip to Startup (C2S) initiative for the project entitled "**A SHAKTI CPU based Smart Vision System on Chip (SoC)**" to be implemented jointly by College of Engineering Trivandrum and M/s Netrasemi Private Limited, Thiruvananthapuram.

Aim of the Project: MeitY recently has announced a semiconductor "Chips to Startup (C2S)" program that not only aims at developing Specialized Manpower in VLSI/Embedded System Design domain but also addresses each entity of the Electronics value chain via Specialized Manpower training, creation of reusable IPs repository, Design of application-oriented Systems/ASICs/FPGAs and deployment by academia/ R&D organization by way of leveraging the expertise available at Start-ups/MSMEs. A joint proposal by College of Engineering Trivandrum (CET) and Netrasemi Private Limited has been selected for the program with central funding under Category-1 (4.7 Crore) for developing an indigenous RISC-V AI/ML chip. The selected candidates will get an opportunity to work on this prestigious project.

Duration: Initial appointment is for one year (contract basis) which is extendable up to the duration of the project.

Eligibility for JRF:

1. **Junior Research Fellow: VLSI Design (5 Nos)**

   Scale of pay: 30000 per month.

   Essential: BTech/BE in EC/EE/AE/EI with CGPA of 8 or more.

   Desirable: MTech/ME in EC/EE/AE/EI, Industry experience of 0-2 years/ Very good knowledge in RTL coding, computer-architecture, SoC design, test and debug. Experience in ASIC/FPGA (preferably FPGA) implementation /

Experience with programming (Verilog/VHDL/C/C++) and scripting languages/tools (Python, Perl, Shell) for design and test automation/ Familiarity with industry standard process lifecycle.

2. **Junior Research Fellow: Embedded Software/System (2 Nos)**

   Scale of pay: 30000 per month.

   Essential: BTech/BE in CS/EC/EE/AE/EI with CGPA of 8 or more.

   Desirable: MTech/ME in CS/EC/EE/AE/EI. / Industry experience of 0-2 years in software development on embedded devices/ Expertise with programming languages such as C /C++. /Very good knowledge of embedded system architecture – ARM / RISCV cores / Knowledge of latest computer architectures with standard as well as high speed peripherals / Knowledge in embedded Linux / RTOS and optimized build process.

   How to apply?

   Interested applicants are requested to download the **application form** and fill in the details.

   Next, register through the **registration** link provided. You need to upload the completed application form with the file name as your full name.

   Last date for submitting the application form is 30th August 2023.

   The applications will be scrutinized and only shortlisted candidates will be intimated through email to appear for an interview.

   The interview will be held at Department of Electronics & Communication Engineering, College of Engineering Trivandrum, tentatively in the first week of September, 2023.